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(54) Method of improving the manufaturing of SOI devices by forming position alignment marks

Verfahren zum Verbessern der Herstellung von SOI-Anordnungen mittels Positions-Ausrichtungsmarken

Procédé pour l'amélioration de la fabrication de dispositifs SOI au moyen de la formation de marques d'alignement de position

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Description

Background of the Invention:

1. Field of the Invention

This invention relates to a method for forming position alignment marks, more particularly for position alignment mark forming which can be useful in the manufacturing of sticked-layer structure SOI (silicon on insulating substrate) devices requiring their silicon layers and back surface electrodes to be laid over and sticked together as they are formed.

2. Description of the Prior Art

In particular, sticked-layer structure SOI devices composed of single-crystal silicon having both of its surfaces sticked to electrodes have decisive advantage in improving and raising to a great degree the circuit integration of their resultant semiconductor LSIs.

Among the drawings attached to this invention, Figs. 1 and 2 and their associates are simplified cross-sectional views of an SOI device of the above-described type, which may make clear its conventionally-employed processing method step by step.

As shown in Fig. 1(a), an SiO_2 film on a silicon (Si) substrate is selectively etched to form a field zone (insulating zone) over the surface of the substrate 11 and is then subjected to thermal oxidation to form thereover a primary insulating layer 12 of oxidized silicon (SiO_2(I)). The silicon substrate thus processed is then, as shown in Fig. 1(b), masked over with a resist 17 and provided with a contact hole 20 which is cut therethrough to link the silicon layer with a back surface electrode later. This contact hole 20 is positioned in an (active) element zone with its position aligned with respect to the end edge of the field zone.

As shown in Fig. 1(c), the silicon substrate is then sticked to poly-silicon (poly-Si) which, through its patterning, forms the back surface electrode 13 in the control hole 20.

As shown in Fig. 2(a) (just a reverse of its position as shown in Fig. 1(c)), the silicon substrate now has its entire surface covered over with a secondary insulating layer (SiO_2 film (II)) 14. In turn, this SiO_2 film (II) 14 is coated with a secondary poly-silicon (poly-Si) layer which is a poly-Si layer 25. After having this layer polished, the silicon base is further sticked to a wafer 22 which forms a bed. The Si substrate 11 is ground and polished from the direction of its top surface (direction shown in the drawing with arrows) and its processing completes when the SiO_2 film (I) 12 is exposed, leaving in its active zone the Si substrate 11 which is now an Si layer. As shown in Fig. 2(b), the Si substrate 11 thereafter has formed thereover a gate insulating film 21 and a poly-Si gate electrode (surface electrode) 16. In this processing, the poly-Si gate electrode has its position aligned with respect to the end edge of the field zone.

According to the conventional manufacturing process as just described in the above, the contact hole 20 as shown in Fig. 1(b) and the poly-Si gate electrode 16 as shown in Fig. 2(b) need to be aligned with each other across the field zone, inevitably necessitating their respective positions to be aligned separately and making their alignment difference vulnerable to increase accordingly. This, in turn, makes it necessary to keep twice as much as allowance for an alignment gap margin between the contact hole 20 and the poly-Si electrode 16 as shown in Fig. 2(b), a fact which hampers the desired high-level circuit integration of SOI devices in a method presented herein as a reference to the prior art in the field the present invention relates to.

Object and Summary of the Invention:

It is an object of the present invention to provide a position alignment method, in the manufacturing of SOI devices, which, making it possible to reduce the required position alignment gap allowance, can serve to realize the high-level circuit integration of such devices simply not made possible today by the conventional technology like one as just explained in the above.

According to an aspect of the present invention there is provided a method for forming a position alignment mark comprising the steps as claimed in the appended claims.

Brief Description of the Drawings:

Figs. 1(a) to 1(c) are cross-sectional views of a conventional SOI device, showing the first half of its processing steps.

Figs. 2(a) and 2(b) are similar cross-sectional views of the conventional SOI device, showing the last half of its processing steps.

Figs. 3(a) to 3(c) are cross-sectional views of an SOI device according to the present invention, showing the first half of its processing steps.

Figs. 4(a) to 4(b) are cross-sectional views of the above SOI device according to the present invention, showing the last half of its processing steps.

Figs. 5(a) to 5(c) are cross-sectional drawings showing in its processing another preferable embodiment of the present invention.

Preferable Embodiments of the Invention:

First described herein below along with Fig. 3 and other drawings associated therewith is an SOI device embodying the present invention and its forming process.

As shown in Fig. 3(a), an SiO_2 film on a Si substrate is selectively etched to form a field zone over the surface of the substrate 1 and is then subjected to thermal oxidization to form thereover a primary insulating layer of

SiO_2 film (I) and with a thickness of 400 to 500 nm. As also shown in Fig. 3(b),

said SiO_2 film (I) 2 is provided with a contact hole 8a for marking its alignment and over an element zone (active zone) a contact hole 8b for a back surface electrode. The contact hole 8a for alignment marking, like the other hole 8b that is for the back surface electrode as just described in the above, passes through the field zone over the SiO_2 film (I) to reach the surface of silicon thereunder (Si substrate 1) with the corresponding part of said insulating layer etched out.

Then, as shown in Fig. 3(c), the poly-Si film as a conductive layer is deposited by CVD to a thickness of 100 to 200 nm. Thus deposited poly-Si as a conductive layer forms through its patterning an alignment marking electrode 3a and a back surface electrode 3b.

As shown in Fig. 4(a) (just a reverse of its position as shown in Fig. 3(c)), the SiO_2 film (II) 4 as a secondary insulating layer is formed to a thickness of 500 to 600 nm over the whole surface of thus formed structure. Over the latter, a poly-Si film 5 is deposited by CVD to a thickness of about 4 μm. After having its surface (the bottom-up direction in the drawing) polished, a wafer as a bed is sticked to the structure each other. The silicon base 1 is then ground from its back surface in a direction shown in the drawing with arrows (from top-down direction in the drawing) till it exposes the bottom of the alignment marking electrode 3a. Then, the latter is ground over its whole surface. All this now leaves the Si substrate 1 still keeping part of its Si layer in the element zone.

After a gate insulating layer 21 of SiO_2 is formed through thermal oxidization as shown in Fig. 4(b), a surface electrode 6 as a transistor gate made of poly-Si is laid thereover in alignment with the alignment mark of a contact pattern completed by then in the form of the alignment marking electrode 3a.

In the above-described embodiment of the present invention, the surface electrode 6 and the contact holes 8a and 8b as shown in Fig. 3(b) need only a single position alignment therebetween, thus making it only necessary to allow for a possible alignment difference margin between them.

Second preferable embodiment of the present invention is now described along with Figs. 5(a) to 5(c). Fig. 5(a) shows that like in the first embodiment of the present invention. The contact hole 8a for position alignment marking is formed in the field zone of the Si substrate and the back surface electrode contact hole 8b is formed in the element zone thereof. In the second embodiment, however, as shown in Fig. 5(a), the poly-Si for plugging is deposited over whole surface of the Si substrate. Over this deposition through CVD, the alignment marking contact hole 8a is etched with the latter kept masked with the resist 7 and then the contact hole 8b is plugged off with the back surface electrode 3b. All this is designed to, in particular, prevent the resultant alignment marking from deformation.

As shown in Fig. 5(c), the Si substrate is again coated over its whole surface with poly-Si which, after its patterning, forms a secondary poly-Si film (II) 15. In the rest of its processing, the second embodiment has no difference with the first embodiment. Namely, like in the first embodiment, the SiO_2 film (II) and the poly-Si film 5 are then formed. After the wafer 10 is sticked to the structure, the Si base 1 is ground till it exposes the alignment marking electrode 3a to form thereon the surface electrode 6.

According to the present invention as just described in the above, it is possible, in the forming and processing of a sticked-layer structure SOI device, to align its electrodes and other constituents directly with its back-side contact pattern. This provides a way for the realization of a sophisticated SOI device with highly-advanced circuit integration not comparable to any which has ever been achieved before.

Making it possible to cut contact holes simultaneously through a surface field (insulating) zone and an element zone on its silicon base, the present invention allows the use of this field zone as the only alignment marking for the formation of its surface electrode and requires only a single alignment. It may be added that poly-silicon is the most recommendable material for SOI devices in any practical application of this invention.

Claims

1. A method for forming a position alignment mark in a SOI semiconductor component manufacturing process comprising the steps of:

   etching part of a front surface of a silicon substrate (1) to form a field zone, the non-etched part of said surface being called element zone;
   forming on said substrate an alignment marking contact hole (8a) and a back surface electrode contact hole (8b), respectively, in said field zone and said element zone;
   forming in said alignment marking contact hole (8a) and said back surface electrode contact hole (8b) an alignment marking electrode (3a) and a back surface electrode (3b), respectively;
   cutting away a silicon layer from the back surface of said silicon substrate (1) to expose said alignment marking electrode (3a) being usable for forming a surface electrode (6) in alignment with said alignment marking electrode (3a).

2. The method of claim 1, comprising the further steps of:
   forming a primary insulating layer (2) over the whole front surface after etching of said part of said front surface; and forming said alignment marking contact hole (8a) exposing said silicon substrate (1) through said primary insulating layer (2) of said field

zone and said back surface electrode contact hole (8b) exposing said silicon substrate (1) through said primary insulating layer (2) of said element zone, respectively.

3. The method of claim 2, wherein said forming of said alignment marking electrode (3a) and said back surface electrode (3b) is accomplished by depositing the whole front surface with a primary poly-Si layer and etching said layer while kept masked said alignment marking contact hole (8a) with a photoresist (7), but the back surface electrode contact hole (8b) remaining plugged with poly-Si; and comprising the further steps of:

removing said photoresist (7);
forming over the whole front surface a patterned secondary poly-Si layer;
forming a SiO_2 layer (4) on said patterned secondary poly-Si layer (15);
depositing a poly-Si film (5) over said SiO_2 layer (4);
sticking a wafer (10) to said poly-Si film (5) after having polished the surface of said poly-Si film (5).

Patentansprüche

1. Verfahren zum Bilden einer Positions-Ausrichtungsmarke bei einem Herstellungsverfahren eines SOI-Halbleiterbauelements mit den Schritten:

Ätzen eines Teils einer Vorderfläche eines Silizium-Substrats (1) um eine Feldzone zu bilden (der nicht geätzte Teil dieser Fläche wird Elementzone genannt);
Bilden eines Ausrichtungsmarkierungs-Kontaktlochs (8a) und eines Rückseitenelektroden-Kontaktlochs (8b) auf dem Substrat in der Feldzone bzw. der Elementzone;
Bilden einer Ausrichtungsmarkierungselektrode (3a) und einer Rückseitenelektrode (3b) im Ausrichtungsmarkierungs-Kontaktloch (8a) bzw. Rückseitenelektroden-Kontaktloch (8b);
Wegschneiden einer Silizium-Schicht von der Rückseite des Silizium-Substrats (1) um die Ausrichtungsmarkierungselektrode (3a) freizulegen, die zum Bilden einer mit der Ausrichtungsmarkierungselektrode (3a) fluchtenden Oberflächenelektrode (6) verwendbar ist.

2. Verfahren nach Anspruch 1 mit den weiteren Schritten:

Bilden einer Primär-Isolierschicht (2) auf der ganzen Vorderfläche nach dem Ätzen des Teils der Vorderfläche; und

Bilden des Ausrichtungsmarkierungs-Kontaktlochs (8a) durch Freilegen des Silizium-Substrats (1) durch die Primär-Isolierschicht (2) der Feldzone hindurch bzw. des Rückseitenelektroden-Kontaktlochs (8b) durch Freilegen des Silizium-Substrats (1) durch die Primär-Isolierschicht (2) der Elementzone hindurch.

3. Verfahren nach Anspruch 2, bei dem das Bilden der Ausrichtungsmarkierungselektrode (3a) und der Rückseitenelektrode (3b) durch Beschichten der ganzen Vorderfläche mit einer Primär-Polysiliziumschicht und Ätzen dieser Schicht durchgeführt wird, wobei das Ausrichtungsmarkierungs-Kontaktloch (8a) mit einem Photoresist (7) bedeckt gehalten, aber das Rückseitenelektroden-Kontaktloch (8b) mit Polysilizium verstopft bleibt; und mit den weiteren Schritten:

Entfernen des Photoresists (7);
Bilden einer gemusterten Sekundär-Polysiliziumschicht auf der ganzen Vorderfläche;
Bilden einer SiO_2-Schicht (4) auf der gemusterten Sekundär-Polysiliziumschicht (15);
Ablagern eines Polysiliziumfilms (5) auf der SiO_2-Schicht (4);
Kleben eines Wafers (10) an den Polysiliziumfilm (5) nachdem die Oberfläche des Polysiliziumfilms (5) poliert wurde.

Revendications

1. Procédé de formation d'une marque d'alignement de position dans un procédé de fabrication de composants à semi-conducteur SOI, comprenant les étapes suivantes :

l'attaque d'une partie d'une surface avant d'un substrat de silicium (1) pour la formation d'une zone de champ, la partie non attaquée de la surface étant appelée "zone d'élément",
la formation sur le substrat d'un trou (8a) de contact de marquage d'alignement et d'un trou (8b) de contact de l'électrode de surface arrière respectivement dans la zone de champ et dans la zone d'élément,
la formation, dans le trou (8a) de contact de marquage d'alignement et dans le trou (8b) de contact d'électrode de surface arrière, d'une électrode (3a) de marquage d'alignement et d'une électrode (3b) de surface arrière respectivement, et
l'enlèvement d'une couche de silicium de la surface arrière du substrat de silicium (1) pour l'exposition de l'électrode (3a) de marquage d'alignement qui peut être utilisée pour la formation d'une électrode (6) de surface dans l'aligne-

ment de l'électrode (3a) de marquage d'alignement.

2. Procédé selon la revendication 1, comprenant les étapes supplémentaires suivantes :

la formation d'une couche isolante primaire (2) sur toute la surface avant après attaque de ladite partie de surface avant, et la formation du trou (8a) de contact de marquage d'alignement exposant le substrat de silicium (1) à travers la couche isolante primaire (2) de la zone de champ et du trou (8b) de contact d'électrode de surface arrière exposant le substrat de silicium (1) à travers la couche isolante primaire (2) de la zone d'élément, respectivement.

3. Procédé selon la revendication 2, dans lequel la formation de l'électrode (3a) de marquage d'alignement et de l'électrode (3b) de surface arrière est réalisée par dépôt sur toute la surface avant d'une couche primaire de silicium polycristallin, et attaque de la couche lorsque le trou (8a) de contact de marquage d'alignement reste masqué par un matériau de réserve photographique (7) mais le trou (8b) de contact de l'électrode de surface arrière restant bouché par le silicium polycristallin, le procédé comprenant les étapes supplémentaires suivantes :

l'enlèvement de la matière de réserve photographique (7),
la formation, sur toute la surface avant, d'une couche secondaire de silicium polycristallin suivant un dessin,
la formation d'une couche de SiO_2 (4) sur la couche secondaire de silicium polycristallin formant un dessin (15),
le dépôt d'un film (5) de silicium polycristallin sur la couche de SiO_2 (4), et
le collage d'une tranche (10) au film (5) de silicium polycristallin après polissage de la surface du film de silicium polycristallin (5).

FIG. 1(a)

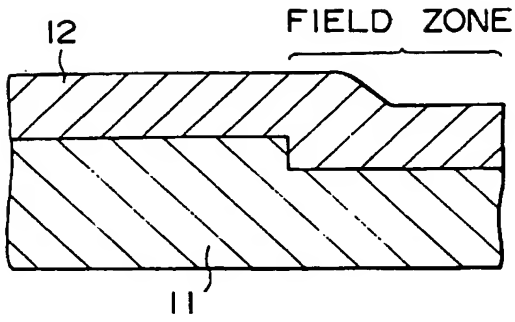

FIG. 1(b)

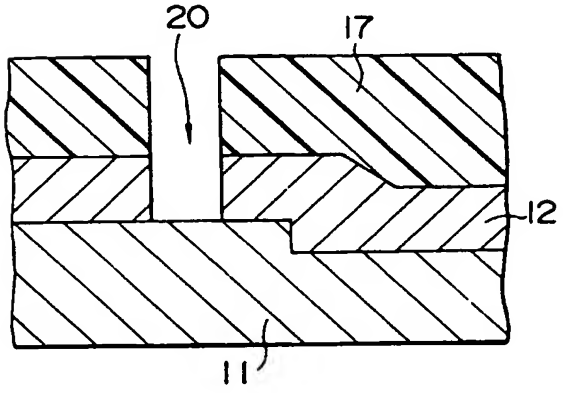

FIG. 1(c)

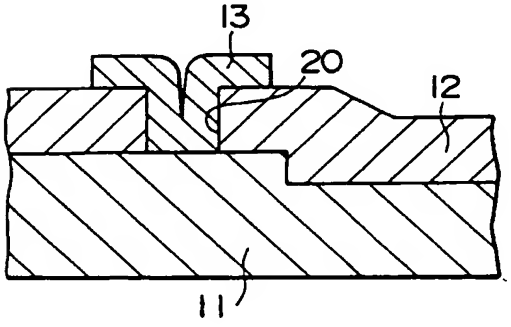

FIG. 2(a)

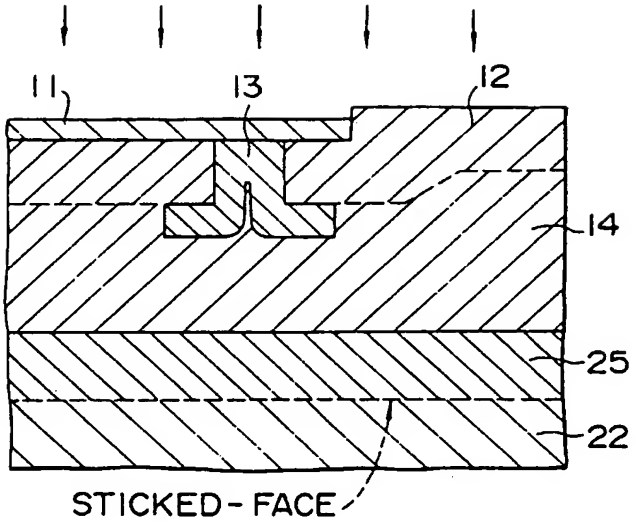

FIG. 2(b)

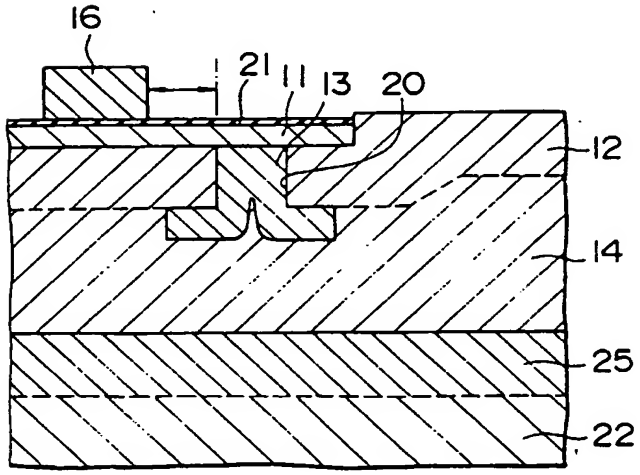

FIG. 3(a)

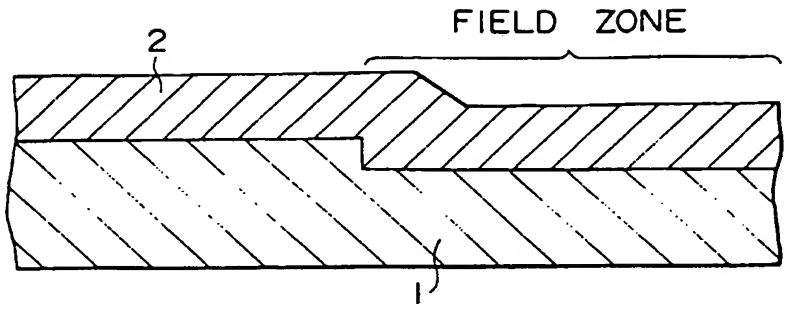

FIG. 3(b)

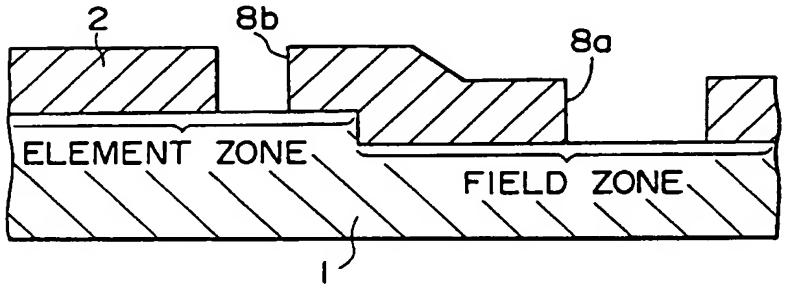

FIG. 3(c)

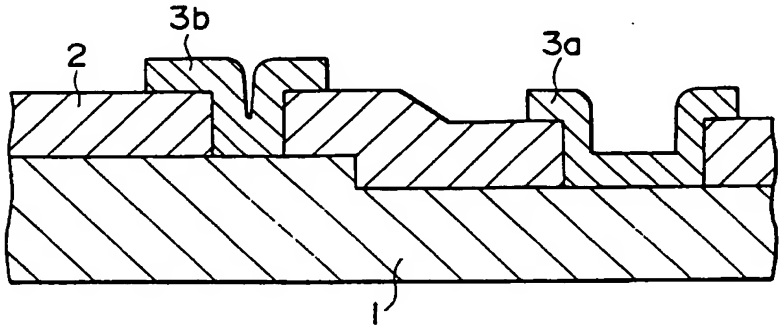

FIG. 4(a)

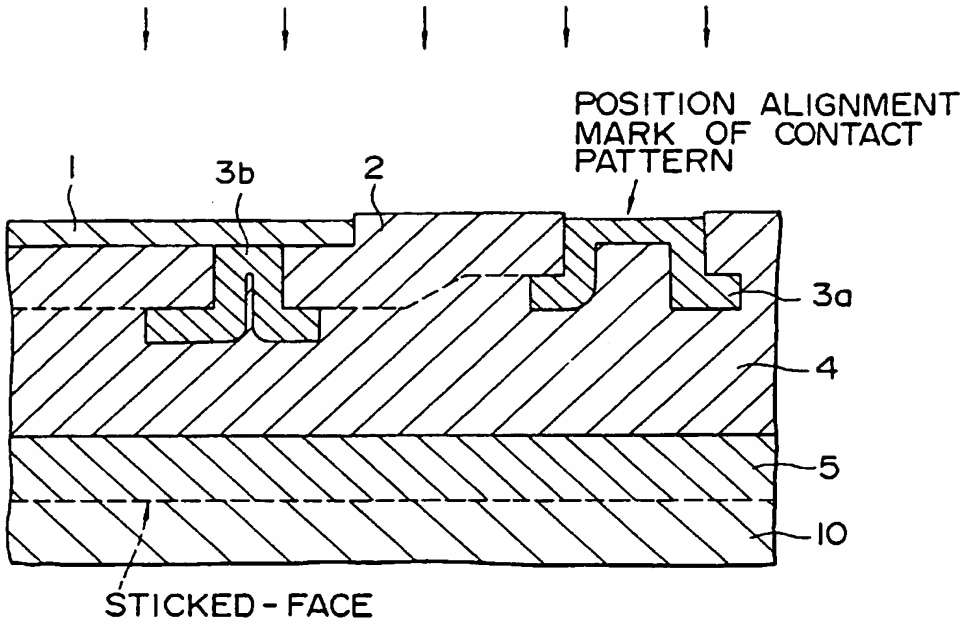
POSITION ALIGNMENT MARK OF CONTACT PATTERN
1
3b
2
3a
4
5
10
STICKED - FACE

FIG. 4(b)

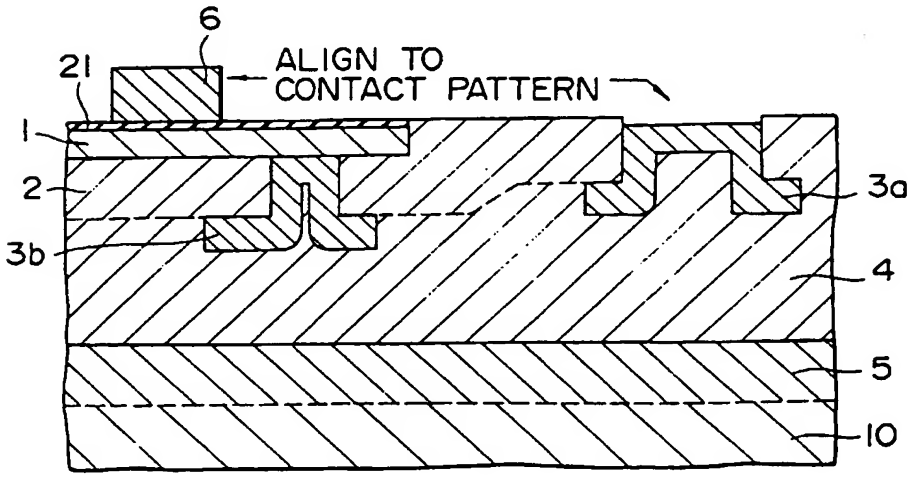
6
21
ALIGN TO CONTACT PATTERN
1
2
3b
3a
4
5
10

FIG. 5(a)

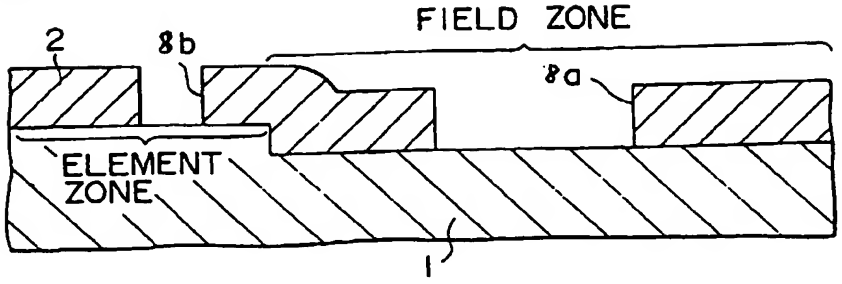

FIG. 5(b)

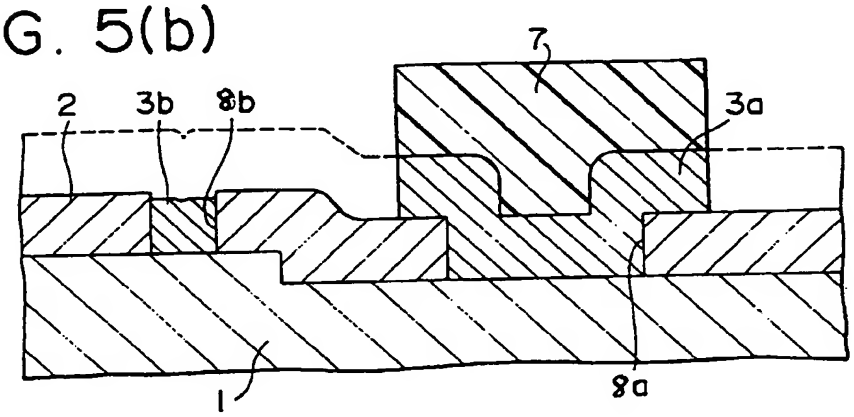

FIG. 5(c)